AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A data processing device formed as a semiconductor integrated circuit to be~~which is~~ coupled to an external device for performing data transmission and reception ~~in synchronization with a clock signal~~, said data processing device comprising:

a central processing unit; and

an interface unit for data transmission and reception to and from the external device,

wherein said interface unit includes:

an external terminal for outputting a~~said~~ clock signal;

an output driver for driving said external terminal to output said clock signal; and

a load circuit capable of imparting, to the clock signal extracted from a~~an arbitrary~~ position in a stage previous to said output driver in a clock signal path, a variable delay in accordance with a delay resulting from an external load coupled to said external terminal in order to generate a ~~said~~ delayed clock signal for latching data inputted from the~~said~~ external device.

2. (previously presented) A data processing device according to claim 1, wherein said load circuit is a time constant circuit comprising resistors and capacitors.

3. (currently amended) A data processing device according to claim 2,

wherein said load circuit comprises a plurality of time constant circuits to generate a plurality of clock signals with different amounts of delay, and ~~by~~ selecting ~~a signal having passed through or not having passed through~~ any of the plurality of clock signals as the delayed~~time constant circuits as a synchronous~~ clock signal for latching the data inputted from the~~said~~ external device.

4. (currently amended) A data processing device formed as a semiconductor integrated circuit to be~~which is~~ coupled to an externala memory device for performing data transmission and reception ~~in synchronization with a clock signal~~, said data processing device comprising:

a central processing unit;

a clock pulse generation circuit capable of~~for~~ generating differen~~a plurality of~~ clock pulse signals; and

an interface unit for data transmission and reception to and from the external memory device~~an external device~~,

wherein said interface unit includes:

a first external terminal for outputting a~~said~~ clock signal derived from a clock pulse signal generated by the clock pulse generation circuit;

an output driver for driving said first external terminal ~~based on the clock signal generated by said clock pulse generation circuit~~ to output said~~the~~ clock signal; and

a load circuit capable of imparting, to the clock signal extracted from a~~an arbitrary~~ position in a stage previous to said output driver in a clock signal path, a variable delay in accordance with a delay resulting from an external load coupled to said first external terminal.

5. (currently amended) A data processing device according to claim 4, further comprising:

a plurality of second external terminals for receiving data from ~~said~~ the external memory device; and

a plurality of latch circuits for latching data received by~~supplied to~~ said plurality of second external terminals,

wherein said latch circuits latch data based on the clock signal as delayed by said load circuit.

6. (currently amended) A data processing device according to claim 4,

wherein each of said clock pulse generation circuit and said latch circuits is~~are~~ constituted by a circuit operating with a first power source voltage, and

wherein each of said output driver and said load circuit is constituted by a circuit operating with a second power source voltage higher than said first power source voltage.

7. (currently amended) A data processing device according to claim 4, wherein said load circuit includes~~is~~ a time constant circuit comprising resistors and capacitors.

8. (currently amended) A data processing device according to claim 4~~7~~,

wherein said load circuit includes a plurality of time constant circuits, ~~and~~ generates a plurality of clock signals with different amounts of delay, and~~by~~ selects~~selecting a signal passing through or not passing through~~ any of the plurality of clock signals~~time constant circuits as a synchronous clock signal~~ for latching data inputted from the external memory~~said external~~ device.

9. (currently amended) A data processing device according to claim 8, wherein said load circuit includes~~further comprising~~:

a selector circuit which selects a~~for selectively transmitting the~~ signal passing through or not passing through any of the plurality of time constant circuits as the clock signal for latching data inputted from the external memory device.

10. (currently amended) A data processing device according to claim 9, further comprising:

a register which stores~~for storing~~ a set value for determining a state of said selector circuit; and

a decoder which generates~~for generating~~ a control signal for said selector circuit in accordance with the set value of the register.

11. (currently amended) An electronic device comprising:

a data processing device as recited in claim 1; and

a nonvolatile memory device capable of coupling to the data processing device,

wherein said nonvolatile memory device performs data transmission and reception based on said clock signal

outputted from said external terminal of said data processing device.